**AXI INFORMATION**

--AXI Reference Guide Xilinx  
<https://www.xilinx.com/support/documentation/ip_documentation/ug761_axi_reference_guide.pdf>

--AXI Basics 1 Introduction to AXI  
<https://support.xilinx.com/s/article/1053914?language=en_US>  
--AXI4-Lite Interface Introduction to AXI4-Lite. Small Introduction but interesant the sequences R/W are describe on the article.  
<https://www.realdigital.org/doc/a9fee931f7a172423e1ba73f66ca4081>

--AXI VERIFICACION IP XILINX  
<https://www.xilinx.com/support/documentation/ip_documentation/axi_vip/v1_1/pg267-axi-vip.pdf>  
  
**AXI IMPLEMENTATION**

--Creating a custom AXI(LITE) IP block in Vivado We can use it to learn how to read register from Microblaze too.  
<https://www.fpgadeveloper.com/2014/08/creating-a-custom-ip-block-in-vivado.html/>

--Proyecto FPGA. Custom IP AXI interface [Spanish Video]  
<https://www.youtube.com/watch?v=6zshglCTV7M&t=409s>

**TESTBENCHES**

--Simulating a Peripheral with AXI4-Lite interface  
<https://www.realdigital.org/doc/32101c99686fe25ec47bedd94e76dc96#step-1-create-a-test-bench-for-the-myled-axi4-lite-custom-ip-core>

--Using the AXI VIP as a master to read and write to an AXI4-Lite slave interface.  
<https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/18842507/Using+the+AXI4+VIP+as+a+master+to+read+and+write+to+an+AXI4-Lite+slave+interface>  
--Validating a master AXI4 interface using the Verification IP as a slave  
<https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/18841614/Validating+a+master+AXI4+interface+using+the+Verification+IP+as+a+slave>  
--AXI Basics 2 – Simulating AXI Interfaces with the AXI Verification IP (AXI VIP)  
<https://support.xilinx.com/s/article/1053935?language=en_US>

--AXI Basics 3 – Master AXI4-Lite simulation with the AXI VIP.  
<https://support.xilinx.com/s/article/1058302?language=en_US>

**ERROR AND DEBUGING ERROR**

--ERROR: [XSIM 43-3217]   
<https://support.xilinx.com/s/question/0D52E00006iHilWSAS/error-xsim-433217-incorrect-project-file-syntax-even-with-a-library-selected?language=en_US>

SUB Módulos: Permite meter dentro de un repos otro repositorio

GIT:

---¿Modelado del motor Teórico? Ver teórico o autotuning